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**Eighth Semester B.E. Degree Examination, May/June 2010**  
**Advanced Computer Architecture**

Time: 3 hrs.

Max. Marks:100

**Note: Answer any FIVE full questions, selecting  
 at least TWO questions from each part.**

**PART - A**

- 1 a. Define computer architecture. Illustrate the seven dimensions of an ISA. (08 Marks)
- b. What is dependability? Explain two main measures of dependability. (06 Marks)
- c. Given the following measurements:  
 Frequency of FP operations = 25%      Average CPI of FP operations = 4.0  
 Average CPI of other instructions = 1.33      Frequency of FPSQR = 2%  
 CPI of FPSQR = 20  
 Assume that the two design alternatives are to decrease the CPI of FPSQR to 2 or to decrease the average CPI of all FP operations to 2.5. Compare the two design alternatives using the processor performance equations. (06 Marks)
- 2 a. With a neat diagram, explain the classic five-stage pipeline for a RISC processor. (10 Marks)
- b. What are the major hurdles of pipelining? Illustrate the branch hazards in detail. (10 Marks)
- 3 a. What are the techniques used to reduce branch costs? Explain both static and dynamic branch prediction used for same. (10 Marks)
- b. With a neat diagram, give the basic structure of Tomasulo based MIPS FP unit and explain the various fields of reservation stations. (10 Marks)
- 4 a. Explain the basic VLIW approach for exploiting ILP, using multiple issues. (10 Marks)
- b. What are the key issues in implementing advanced speculation techniques? Explain them in detail. (10 Marks)

**PART - B**

- 5 a. Explain the basic schemes for enforcing coherence in a shared memory multiprocessor system. (10 Marks)
- b. Explain the directory based coherence for a distributed memory multiprocessor system. (10 Marks)
- 6 a. Assume we have a computer where the clocks per instruction (CPI) is 1.0 when all memory accesses hit in the cache. The only data accesses are loads and stores and these total 50% of the instructions. If the miss penalty is 25 clock cycles and the miss rate is 2%, how much faster would the computer be if all instructions were cache hits? (10 Marks)
- b. Explain in brief, the types of basic cache optimization. (10 Marks)
- 7 a. Which are the major categories of advanced optimizations of cache performance? Explain any one in detail. (10 Marks)
- b. Explain in detail, the architecture support for protecting processes from each other via virtual memory. (10 Marks)
- 8 a. Explain in detail, the hardware support for preserving exception behaviour during speculation. (10 Marks)
- b. Explain the prediction and speculation support provided in IA64. (10 Marks)

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## Eighth Semester B.E. Degree Examination, December 2010 Advanced Computer Architecture

Time: 3 hrs.

Max. Marks:100

**Note: Answer any FIVE full questions, selecting  
 at least TWO questions from each part.**

### PART – A

1 a. List and explain four important technologies, which have led to the improvements in computer system. (07 Marks)

b. The given data presents the power consumption of several computer system components:

| Component  | Product            | Performance | Power                    |
|------------|--------------------|-------------|--------------------------|
| Processor  | Sun Niagara 8-core | 1.2 GHz     | 72-79 W                  |
| DRAM       | Kingston 1 GB      | 184 – pin   | 3.7 W                    |
| Hard drive | Diamond Max        | 7200 rpm    | 7.9 W read<br>4.0 W idle |

i) Assuming the maximum load for each component, a power supply efficiency of 70%, what wattage must the server's power supply deliver to a system with a Sun Niagara 8-core chip, 2 GB 184-pin Kingston DRAM and 7200 rpm hard drives?

ii) How much power will the 7200 rpm disk drive consume, if it is idle roughly 40% of the time?

iii) Assume that for the same set of requests, a 5400 rpm disk will require twice as much time to read data as a 10800 rpm disk. What percentage of time would the 5400 rpm disk drive be idle to perform the same transaction as in part (ii)? (07 Marks)

c. We will run two applications on dual Pentium processor, but the resource requirements are not the same. The first application needs 80% of the resources, and the other only 20% of the resources.

i) Given that 40% of the first application is parallelizable, how much speed up will we achieve with that application, if run in isolation?

ii) Given that 99% of the second application is parallelizable, how much speed up will this application observe, if run in isolation?

iii) Given that 40% of the first application is parallelizable, how much overall system speedup would you observe, if we parallelized it? (06 Marks)

2 a. List pipeline hazards. Explain any one in detail. (07 Marks)

b. List and explain five different ways of classifying exception in a computer system. (07 Marks)

c. An unpipelined machine has 10 ns clock cycle and it uses four cycles for ALU operations and branches, five cycles for memory operations. Assume that relative frequencies of these operations are 40%, 20% and 40% respectively. Suppose due to clock skew and set up, pipelining the machine adds 1 ns overhead to the clock. Find the speed up from pipelining. (06 Marks)

3 a. Show how the below loop would look on MIPS 5-stage pipeline, under the following situations. Find the number of cycles per iteration, for each case. Assume the latencies for integer and floating point operations, as given in the prescribed text book.

Loop : L . D        F0, 0(R1)  
           ADD . D     F4, F0, F2  
           S . D        F4, 0(R1)  
           DADDUI    R1, R1, # - 8  
           BNE        R1, R2, loop

**Question No.3(a) continued...**

- i) Without scheduling and without loop unrolling.  
 ii) With scheduling and without loop unrolling.  
 iii) With loop unrolling four times and without scheduling.  
 iv) With loop unrolling four times and with scheduling. (12 Marks)
- b. What is the drawback of 1-bit dynamic branch prediction method? Clearly state, how it is overcome in 2-bit prediction. Give the state transition diagram of 2-bit predictor. (08 Marks)
- 4 a. Explain the salient features of VLIW processor. (08 Marks)  
 b. Explain branch-target buffer. (08 Marks)  
 c. Write a short note on value predictors. (04 Marks)

**PART – B**

- 5 a. What is multiprocessor cache coherence? List two approaches to cache coherence protocol. Give the state diagram for write-invalidate write-back cache coherence protocol. Explain the three states of a block. (12 Marks)  
 b. List and explain any three hardware primitives to implement synchronization. (08 Marks)
- 6 a. Assume we have a computer where CPI is 1.0 when all memory accesses hit in the cache. The only data accesses are loads and stores, and these total 50% of the instructions. If the miss penalty is 25 cycles and miss rate is 2%, how much faster would the computer be, if all instructions were cache hits? (08 Marks)  
 b. Briefly explain four basic cache optimization methods. (12 Marks)
- 7 a. List and explain three C's model that sorts all cache misses. (06 Marks)  
 b. Explain the optimization methods mentioned below :  
 i) Trace cache to reduce hit time  
 ii) Non-blocking cache to increase cache bandwidth  
 iii) Multi banked cache to increase cache bandwidth. (09 Marks)  
 c. Briefly explain how memory protection is enforced via virtual memory. (05 Marks)
- 8 a. Consider the loop below:  
 for (i = 1 ; i ≤ 100 ; i = i + 1) {  
     A [ i ] = A [ i ] + B [ i ] ; 1 \* S1 \* 1  
     B [ i + 1 ] = C [ i ] + D [ i ] ; 1 \* S2 \* 1  
 }  
 What are the dependences between S1 and S2? Is this loop parallel? If not, show how to make it parallel. (08 Marks)  
 b. Explain Intel IA-64 architecture. (12 Marks)

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