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06CS81

Eighth Semester B.E. Degree Examination, June/July 2011
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions each from Part – A and Part - B.***

PART – A

1 a. Explain with a learning curve, how the cost of processor varies with time along with factors influencing the cost. **(06 Marks)**

b. Find the number of dies per 200cm wafer of circular shape that is used to cut die that is 1.5cm side and compare the number of dies produced on the same wafer if die is 1.25cm. **(06 Marks)**

c. Define Amdahls law. Derive an expression for CPU clock as a function of instruction count, clocks per instruction and clock cycle time. **(08 Marks)**

2 a. What are major hazards in a pipeline? Explain data hazard and methods to minimize data hazard with example. **(08 Marks)**

b. Consider the following calculations : $x = y + z$; $a = b * c$. Assume the calculations are done using registers. Show, using 5 stage pipeline, how many clock pulses are required for direct operations. By recording with stalls show how many clock pulses are required and saving in the number of clock pulses to solve data hazard. **(12 Marks)**

3 a. What are data dependencies? Explain name dependences with example between two instructions. **(06 Marks)**

b. What is correlating predictors? Explain with examples. **(06 Marks)**

c. For the following instructions, using dynamic scheduling show the status of R.O.B, Reservation station when only MUL.D is ready to commit and two L.D committed.

```
L.D   F6, 32(R2)
L.D   F2, 44(R3)
MUL.D  F0, F2, F4
SUB.D  F8, F2, F6
DIV.D  F10, F0, F6
ADD.D  F6, F8, F2.
```

Also show the type of hazards between instructions. **(08 Marks)**

4 a. Explain the basic VLIW approach for exploiting ILP, using multiple issues. **(08 Marks)**

b. What are the key issues in implementing advanced speculation techniques? Explain in detail. **(08 Marks)**

c. Write a note on value predictors. **(04 Marks)**

PART – B

5 a. Explain the directory based cache coherence for a distributed memory multi processor system along with state transition diagram. **(10 Marks)**

b. Explain any two hardware primitives to implement synchronization with example. **(10 Marks)**

6 a. Explain block replacement strategies to replace a block, with example when a cache **(06 Marks)**

b. Explain the types of basic cache optimization. **(09 Marks)**

c. With a diagram, explain organization of data cache in the opteron microprocessor. **(05 Marks)**

7 a. Explain the following advanced optimization of cache :
i) Compiler optimizations to reduce miss rate.
ii) Merging write buffer to reduce miss penalty.
iii) Non blocking caches to increase cache band width. **(09 Marks)**

b. Explain in detail the architecture support for protecting processor from each other via virtual machines. **(06 Marks)**

c. Explain internal organization of 64Mb DRAM. **(05 Marks)**

8 a. Explain in detail the hardware support for preserving exception behaviour during speculation. **(10 Marks)**

b. Explain the architecture of IA64 intel processor and also the prediction and speculation support provided. **(10 Marks)**

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Eighth Semester B.E. Degree Examination, December 2011
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Define the computer architecture. Explain the response time, throughput, elapsed time and processor clock. **(06 Marks)**

b. Briefly explain the Amdahl's law. **(07 Marks)**

c. Two code sequences for a particular machine are considered by a compiler designer.

Instruction class	CPI for this instruction class
A	1
B	2
C	3

The compiler designer considers 2 code sequences that require the following instruction counts for a particular high – level language statement.

Code sequence	Instruction counts for instruction class		
	A	B	C
1	20	10	20
2	40	10	10

i) Which code sequence executes most of the instructions?
ii) What is the CPI for each sequence?
iii) Which will be faster? **(07 Marks)**

2 a. What are the major hurdles of pipelining? Illustrate the data hazard, briefly. **(10 Marks)**

b. With a neat block diagram, explain how an instruction can be executed in 4 or 5 clock cycles in MIPS data path, without the pipeline register. **(10 Marks)**

3 a. List the steps to unroll the code and schedule. **(05 Marks)**

b. Explain how Tomasulo's algorithm can be extended to support speculation. **(10 Marks)**

c. Explain the dynamic branch prediction state diagram. **(05 Marks)**

4 a. Explain the basic VLIW approach. List its drawbacks. **(08 Marks)**

b. With a neat diagram, explain the steps involved in handling an instruction, with a branch target buffer. Also evaluate how well it works. **(12 Marks)**

PART – B

5 a. Explain the different taxonomy of parallel architecture. **(08 Marks)**

b. With a neat diagram, explain the basic structure of a centralized shared – memory and distributed – memory multiprocessor. **(06 Marks)**

c. Explain the snooping, with a respect to cache – coherence protocols. **(06 Marks)**

6 a. Explain the six basic optimizations. **(12 Marks)**

b. With a neat diagram, explain the hypothetical memory hierarchy. **(08 Marks)**

7 a. Explain the DRAM technology. How do you improve memory performance inside a DRAM chip? **(10 Marks)**

b. Explain the compiler optimizations to reduce miss rate. **(10 Marks)**

8 a. Find all the true dependences, output dependences and antidependences and eliminate the output and antidependences by renaming, in the code given below:

```
for (i = 1;   i <= 100;  i = i + 1) {
    y[i] = x[i] /c ;      /* s1 */
    x[i] = x[i]+c ;       /* s2 */
    z[i] = y[i]+c ;       /* s3 */
    y[i] = c – y[i] ;     /* s4 */
    }
```

(10 Marks)

b. Write short notes on:

i) The Itanium 2 processor

ii) IA – 64 register model. **(10 Marks)**

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