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Third Semester B.E Degree Examination, Dec. 07 / Jan. 08
Logic Design

Time: 3 hrs.

Max. Marks:100

Note : Answer any FIVE full questions choosing at least TWO questions from each part..

PART - A

- 1
 - a. Using Karnaugh map simplify the following Boolean expression and give the implementation of the same using :
 i) NAND gates only (SOP form) ii) NOR gates only (POS form)
 $f(A, B, C, D) = \sum m(0, 1, 2, 4, 5, 12, 14) + dc(8, 10)$. (08 Marks)
 - b. Find the prime implicants for the Boolean expression using Quine Mc Clusky's method.
 $F(w, X, Y, Z) = \sum m(1, 3, 6, 7, 8, 9, 10, 12, 13, 14)$. (10 Marks)
 - c. Explain the principle of duality. (02 Marks)

- 2
 - a. Realize the Boolean expression $f(w, x, y, z) = \sum m(4, 6, 7, 8, 10, 12, 15)$ using a 4 to 1 line multiplexer and external gates. (08 Marks)
 - b. Design a 1-bit comparator using basic gates. (05 Marks)
 - c. Implement the following Boolean functions using an appropriate PLA.
 $F1(A, B, C) = \sum m(0, 4, 7)$; $F2(A, B, C) = \sum m(4, 6)$. (04 Marks)
 - d. What are the three different models for writing a module body in Verilog HDL. Give an example for any one model. (03 Marks)

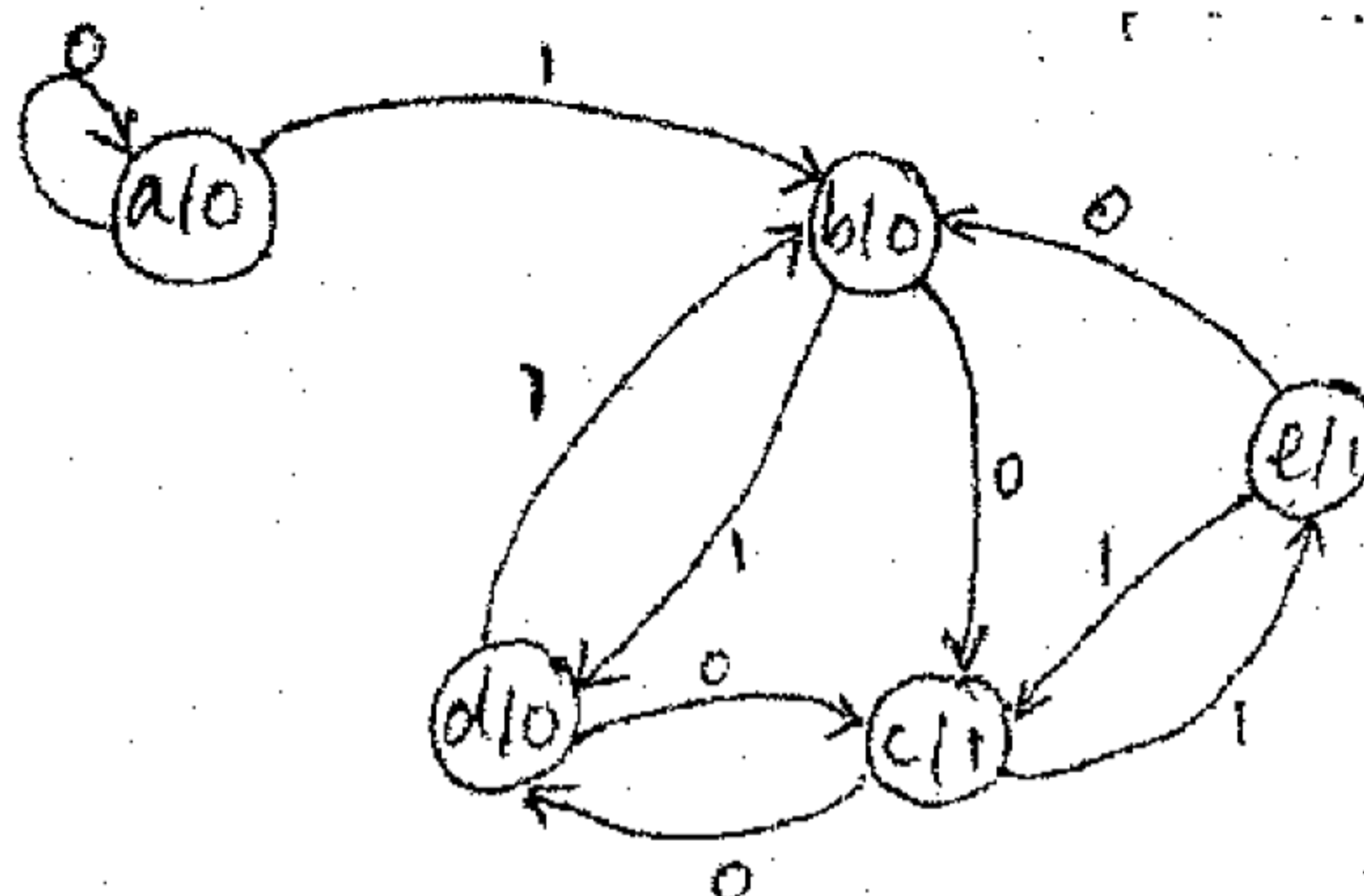
- 3
 - a. Explain with example the 2's complement arithmetic using all the cases. (04 Marks)
 - b. Draw a block diagram of a 4 – bit adder – subtract circuit using full adder and give a brief description. (04 Marks)
 - c. Design a 2-bit fast adder. Give its implementation using gates. (08 Marks)
 - d. Write a HDL code for a full adder. (04 Marks)

- 4
 - a. Write the characteristic of an ideal clock. (06 Marks)
 - b. With the help of a block diagram, explain the working of a JK Master – Slave flip – flop. (08 Marks)
 - c. Show how a SR flip – flop can be converted to a JK flip – flop. (06 Marks)

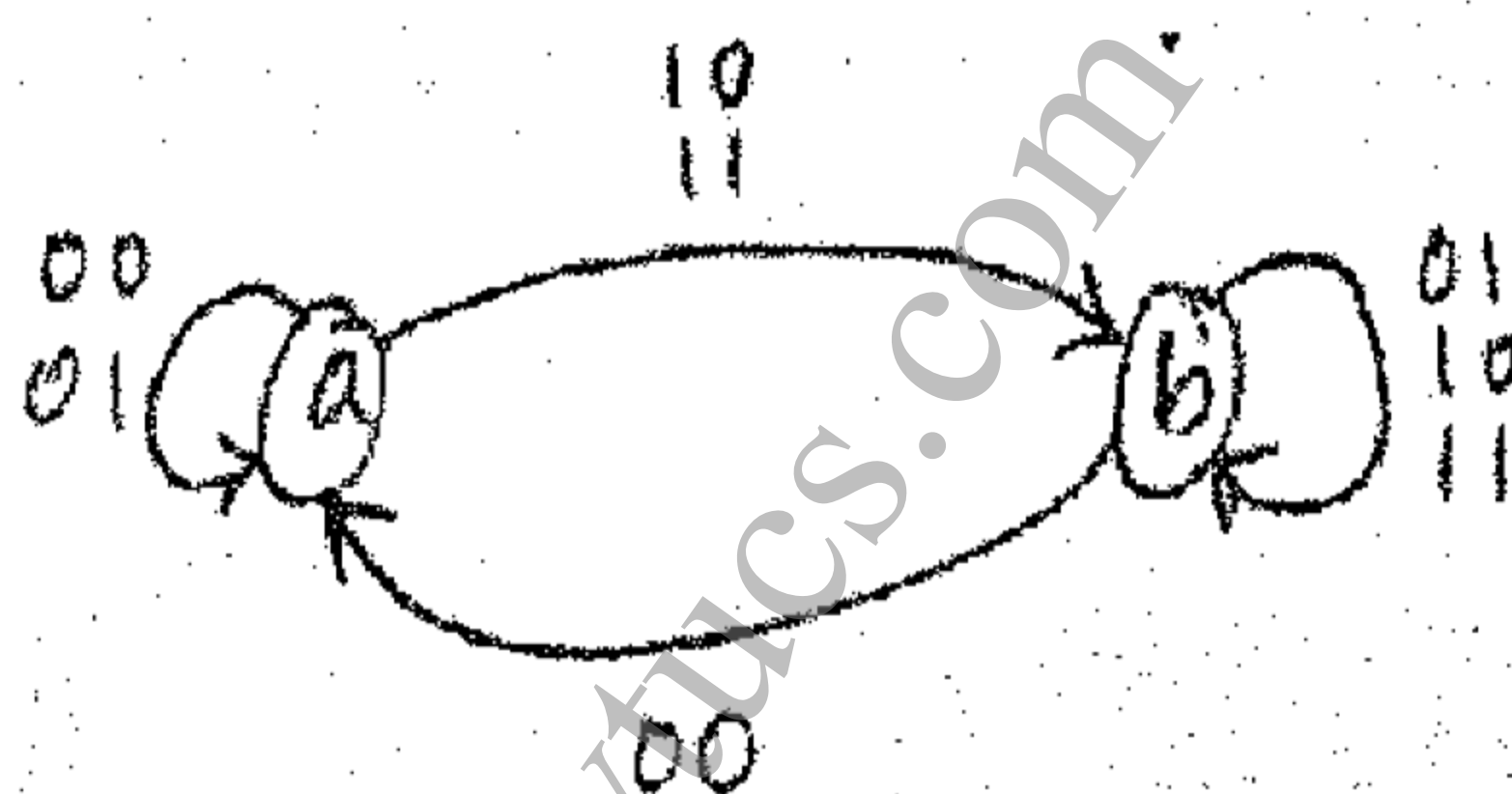
PART - B

- 5
 - a. Distinguish between a ring counter and a Johnson counter. (04 Marks)
 - b. Explain the working of a 3-bit asynchronous down counter. (06 Marks)
 - c. Design a synchronous mod – 5 up counter using JK flip – flop. Give excitation table of JK flip – flop, state diagram and state table. (10 Marks)

- 6 a. Explain the difference between Mealy and Moore models. (04 Marks)
 b. Reduce the state transition diagram by row elimination method and implication table method.



- c. Design an asynchronous sequential logic circuit for the state transition diagram shown. (10 Marks)



(06 Marks)

- 7 a. Draw a 4-bit D/A converter using R/2R resistors and explain its working. (10 Marks)
 b. Explain the A/D converter by simultaneous conversion. Draw the block diagram of a 2-bit simultaneous A/D converter. (10 Marks)
- 8 a. With the aid of a circuit diagram, explain the operation of a 2-input TTL NAND gate with totem-pole output. (08 Marks)
 b. Explain the operation of a 2-input CMOS NOR gate with a help of a circuit diagram. (06 Marks)
 c. Write a note on the CMOS characteristics. (06 Marks)
