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Third Semester B.E. Degree Examination, June / July 08
Logic Design

Time: 3 hrs.

Max. Marks:100

Note : Answer any FIVE full questions, choosing atleast two from each part.

PART - A

- 1 a. What are universal gates? Implement the following function using universal gates only
 $((A+B)C)D$ (04 Marks)
- b. Simplify the following using K - map $F(A,B,C,D) = \overline{ABC} + AD + \overline{BD} + \overline{CD} + \overline{AC} + \overline{AB}$. (06 Marks)
- c. What are the drawbacks of k-map? Simplify the following expression using Quine - Mc Clusky Method. $F(A,B,C,D) = \Sigma(1,2,8,9,10,12,13,14)$. (10 Marks)
- 2 a. Show that using a 3 - to - 8 decoder and multi -input OR gate. The following Boolean expressions can be realized.
 $F_1(A,B,C) = \Sigma m(0,4,6)$, $F_2(A,B,C) = \Sigma m(0,5)$, $F_3(A,B,C) = \Sigma m(1,2,3,7)$. (04 Marks)
- b. Design Decimal - to - BCD encoder? (04 Marks)
- c. What are the different types of PLD's and implement the 7 - segment decoder using PLA? (08 Marks)
- d. Write a verilog code for 4 : 1 multiplexer using case statement. (04 Marks)
- 3 a. i) Perform 8 - bit addition of the decimal numbers - 28 and + 15 in 2's complement.
ii) Perform 8 - bit subtraction of the decimal numbers - 28 and + 65 in 2's complement. (06 Marks)
- b. i) Find the binary addition of $(7510)_{10}$ and $(538)_{10}$ using 16 - bit numbers.
ii) Find the binary subtraction of $(200)_{10}$ and $(125)_{10}$ using 8 - bit numbers. (10 Marks)
- c. Explain the binary Adder - subtracted circuit with an example. (04 Marks)
- 4 a. What is Schmitt trigger? Explain Schmitt trigger transfer characteristic. (10 Marks)
- b. Explain the different types of flip fops along with their truth table. Also explain the race - around condition in a flip flop. (10 Marks)
- c. Differentiate between combinational circuit and sequential circuit. (10 Marks)

PART - B

- 5 a. Explain a 4 -bit serial input shift registers in detail and give its timing diagram. (10 Marks)
- b. Design a mod - 5 synchronous up counter using JK flip flop. (10 Marks)
- 6 a. Explain Moore model with state synthesis table and also obtain the circuit diagram for Moore model. (10 Marks)
- b. Design an asynchronous sequential logic circuit for state transition diagram shown in Fig. Q 6(b).

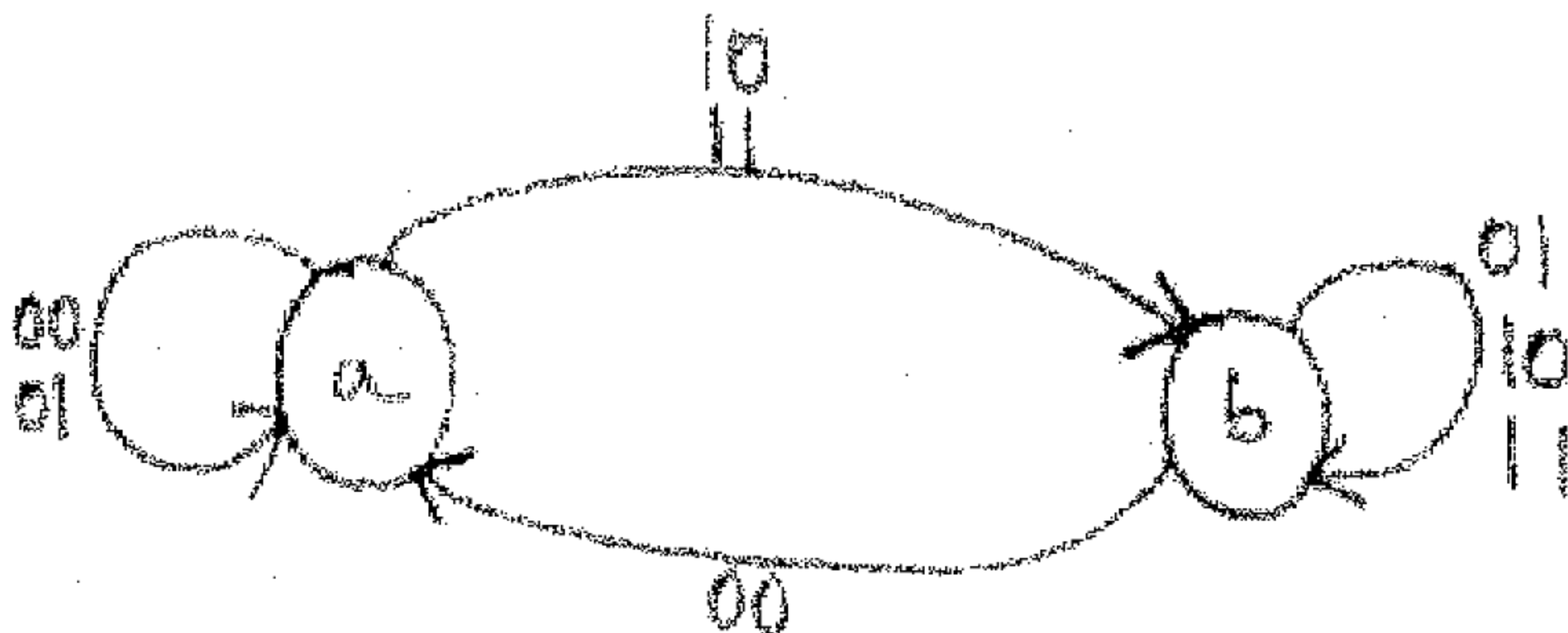


Fig. Q 6(b)

- a. What is a binary ladder? Explain the binary ladder with a digital input of 1000. (10 Marks)
- b. Explain a 2 - bit simultaneous A/D converter. (10 Marks)
- a. With a circuit diagram, explain the operation of the CMOS NAND gate. (10 Marks)
- b. Explain a 2 - input NAND gate TTL with Totem - pole output with a neat diagram. (10 Marks)
