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06CS33

Third Semester B.E. Degree Examination, May/June 2010
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Simplify the given Boolean function by using K-map method and express it in SOP form. Realise logic circuit by using NAND gates only.
$f(A, B, C, D) = \sum(m(7, 9, 10, 11, 12, 13, 14, 15))$ **(06 Marks)**

b. Simplify following Boolean function by using K-map method in POS form:
$f(A, B, C, D) = \sum m(0, 1, 2, 3, 4, 5, 7)$ **(06 Marks)**

c. Find prime implicants for the Boolean expression by using Quine McClusky method.
$f(A, B, C, D) = \sum(1, 3, 6, 7, 8, 9, 10, 12, 14, 15) + d(11, 13)$ **(08 Marks)**

2 a. Define decoder. Draw logic diagram of 3:8 decoder with enable input. **(06 Marks)**

b. Implement the given Boolean function by using 8:1 multiplexer.
$f(A, B, C, D) = \sum(0, 1, 3, 5, 7, 11, 12, 13, 14)$ **(06 Marks)**

c. With a neat diagram, explain the decimal to BCD encoder. **(08 Marks)**

3 a. What are the three different models for writing a module body in verilog HDL? Give example for any one model. **(06 Marks)**

b. With truth table and a neat logic diagram, explain full adder implementation. **(06 Marks)**

c. Explain how IC 7483 can be used as 4 bit adder/subtractor. **(08 Marks)**

4 a. With transfer characteristic, explain how Schmitt trigger converts a random waveform into a rectangular waveform. **(06 Marks)**

b. Explain basic S.R flip-flop by using NOR gate. What is the drawback of S-R flip-flop? How J-K flip-flop is obtained from S-R flip-flop? **(08 Marks)**

c. Find out characteristic equations of J-K flip-flop and D flip-flop. **(06 Marks)**

PART – B

5 a. Explain any two types of shift register with waveforms. How Johnson counter is obtained from shift register? **(10 Marks)**

b. Design Mod-6 synchronous counter by using J-K flip-flop. Give excitation table of J-K flip-flop, state diagram and state transition table. **(10 Marks)**

6 a. Differentiate between Moore and Mealy model of synchronous sequential circuit. **(04 Marks)**

b. Reduce the state transition diagram of Mealy model by row elimination method and implication table method. **(16 Marks)**

State transition diagram.

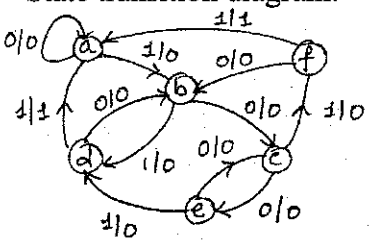

Fig. Q6 (b)

7 a. Explain with neat diagram, R-2R ladder type 4 bit D to A converter. Find out analog output if input is 1100 and '1'= +5 volts. For 10 bit DAC if full scale output is 10.24 volts, what is resolution? **(10 Marks)**

b. Explain with a neat diagram, successive approximation type DAC. **(10 Marks)**

8 a. With a neat circuit diagram, explain the operation of a two input TTL NAND gate with tolem pole output. **(08 Marks)**

b. Explain with a neat diagram, CMOS inverter. **(06 Marks)**

c. Explain CMOS characteristics. **(06 Marks)**

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06CS33

Third Semester B.E. Degree Examination, December 2010

Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Draw the logic circuit whose Boolean equation is $Y = \overline{A + B} + \overline{C}$, use only NAND gates. **(04 Marks)**

b. Find the minimal sum and minimal product using Karnaugh map.

$$f(a,b,c,d) = \sum m(6,7,9,10,13) + d(1,4,5,11)$$ **(08 Marks)**

c. Find the prime implicants for the following function using Quine Mccluskey method:

$$f(a,b,c,d) = \sum m(1,2,8,9,10,12,13,14)$$ **(08 Marks)**

2 a. Implement the following function using a 8 : 1 multiplexer :

$$f(a,b,c,d) = \sum m(0,1,5,6,8,10,12,15)$$ **(05 Marks)**

b. Describe the working principle of a 3 : 8 decoder. Realize the following Boolean expressions using the 3 : 8 decoder :

$$F_1(A,B,C) = \sum m(1,2,3,4) \qquad F_2(A,B,C) = \sum m(3,5,7)$$ **(06 Marks)**

c. What is PLA? How does PLA differ from PAL? **(05 Marks)**

d. Write HDL code for a 4 to 1 Mux considering any model. **(04 Marks)**

3 a. How is 2's complement representation used to perform subtraction? Give an example. **(04 Marks)**

b. Show how two 7483 can be used to add/subtract two 8 bit numbers. Draw a neat diagram and explain its working. **(08 Marks)**

c. Design a 2 bit fast adder. Give its implementation using gates. **(08 Marks)**

4 a. Calculate the clock cycle time for a system that uses a clock, that has a frequency of :
i) 10 MHz ii) 6 MHz iii) 750 KHz **(03 Marks)**

b. With a neat block diagram, explain the working of a Master-Slave JK flip flop. Also write its truth table. **(07 Marks)**

c. Explain the function of the circuit shown here with the state transition diagram. **(10 Marks)**

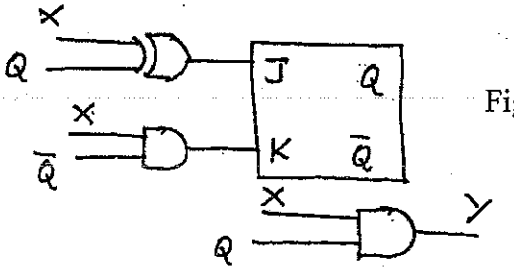

Fig.Q4(c)

PART – B

5 a. Draw the logic diagram of a 4 bit serial in serial out shift register using JK flip flop and explain its working with an example. **(05 Marks)**

b. Give the HDL code for a shift register of 5 bits constructed using D flip flops. **(03 Marks)**

c. Construct a mod 8 asynchronous counter and write the truth table and draw waveforms. **(06 Marks)**

d. Design a mod 4 synchronous counter using a –ve edge triggered JK flip flop. Draw the state transition diagram. **(06 Marks)**

6 a. For the following state transition diagram, design equations for Moore model and generate the circuit diagram. **(10 Marks)**

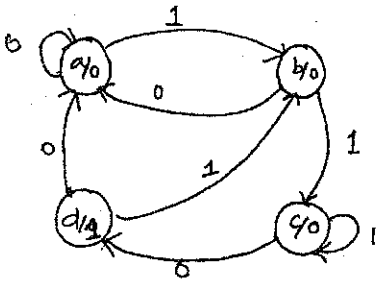

Fig.Q6(a)

b. Design an asynchronous sequential logic circuit for state transition diagram shown below:

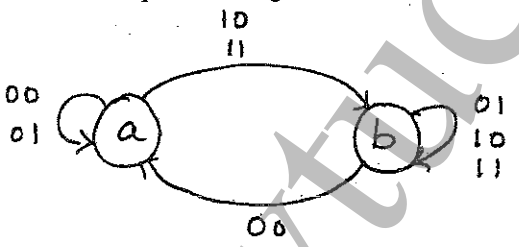

Fig.Q6(b)

(06 Marks)

c. How does state transition diagram of a Moore machine differ from Mealy machine? **(04 Marks)**

7 a. Draw a binary ladder network for a digital input 1000 and obtain its equivalent circuit. **(06 Marks)**

b. Explain the concept of "successive approximation" of a A/D converter. **(08 Marks)**

c. In a 8 bit counter type A/D converter driven by 500 KHz clock, find :

i) Conversion time
ii) Average conversion time
iii) Maximum conversion time. **(06 Marks)**

8 a. Explain the working of CMOS NAND, NOR gates. **(08 Marks)**

b. Explain with a neat diagram, working of a 2 input NAND gate TTL with totempole output. **(07 Marks)**

c. Explain how transistor acts as a switch. Define power dissipation and propagation delay time. **(05 Marks)**

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