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10CS33

Third Semester B.E. Degree Examination, Dec. 2013/Jan. 2014
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. With the aid of the circuit diagram, explain the operation of 2 – input TTL NAND gate. **(08 Marks)**

b. What are universal gates? Implement the following function using universal gates only $\left(\overline{(A+B)C}\right)D$. **(06 Marks)**

c. Write the truth table of the logic circuit having 3 input A, B and C and output output expressed as $y = A\bar{B}C + ABC$. Also simplify the expression using Boolean expression and implement the logic circuit using NAND gates? **(06 Marks)**

2 a. Using Q – M method, simplify the expressions f(A, B, C, D) = Σ(0, 3, 5, 6, 7 11, 14). Write the gate diagram for the simplified expression using NAND – NAND gates. **(10 Marks)**

b. A digital system is to be designed in which the month of the year is given as input is four bit form. The month January is represented as '0000' February '0001' and so on. The output of the system should be '1' corresponding to the input of the month containing 31 days or otherwise it is '0' consider the excess numbers in the input beyond '1011' as don't care conditions for system of four variables (A, B, C, D) find the following :

i) Boolean expression in Σm and πm form
ii) Write the truth table
iii) Using K – map, simplify the Boolean expression of canonical minterm form
iv) Implement the simplified equation using NAND – NAND gates. **(10 Marks)**

3 a. Write a 4: 1 MUX verilog program using conditional 'assign' and 'case' statement. **(06 Marks)**

b. What are static hazards? How to design hazards free circuit? Explain with an example. **(06 Marks)**

c. Explain IV – bit magnitude comparator. **(08 Marks)**

4 a. Draw the logic diagram of clock D – flip/flop write its truth table and characteristic equation, state diagram and excitation table, what is the draw back JK flip/flop. **(10 Marks)**

b. Differentiate between combinational circuit and sequential circuits. **(05 Marks)**

c. Show how a SR flip/flop can be converted into T – flip/flop. **(05 Marks)**

PART – B

5 a. Using negative edge triggered JK flip/flop, draw the logic diagram of a 4-bit serial-in-serial-out shift register. Draw the waveform to shift the binary number 1010 into this register. Also draw the waveform for 4 clock transistor when J = K = 0. **(08 Marks)**

b. Explain the working of mod – 4 ring counter. **(06 Marks)**

c. Explain with a neat diagram, how shift register can be applied for serial addition. **(06 Marks)**

6 a. With the help of neat block diagram and timing diagram, explain the working of a mod -16 ripple counter constructed using the edge triggered JK- flip/flop. **(08 Marks)**

b. Design asynchronous counter for the sequence $0 \rightarrow 4 \rightarrow 1 \rightarrow 2 \rightarrow 6 \rightarrow 0 \rightarrow 4$, using SR flip-flop. **(12 Marks)**

7 a. Design a sequence detector that receives bindery data stream as its input, X and signals when a combinations '011' arrives at the input by making its output, Y high which otherwise remain line consider data is coming from left, i. e the first bit to be identified is 1. Second 1 and third 0 from the input sequence. Design mealy model? **(14 Marks)**

b. Realize the sequential circuit for the state diagram. **(06 Marks)**

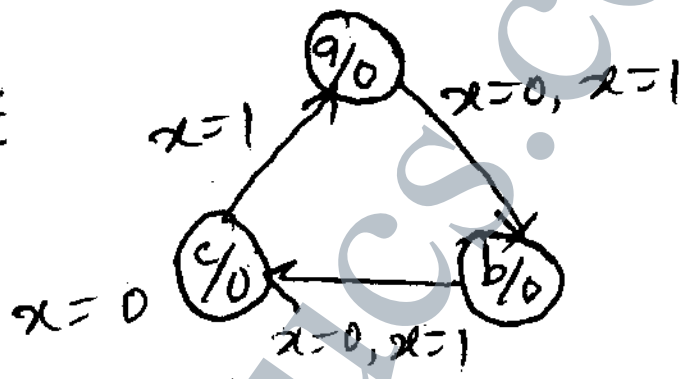

Fig. Q7(b)

8 a. Explain 2-bit simultaneous A/D converter. **(10 Marks)**

b. What is binary ladder? Explain the binary ladder with a digital input of 1000. **(06 Marks)**

c. What is accuracy and resolution of the D/A converter? What is the resolution of a 12 bit D/A converter which uses binary ladder? If the full scale output is + 10 V, what is the resolution in volts? **(04 Marks)**

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