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10CS33

Third Semester B.E. Degree Examination, June/July 2013
Logic Design

Time: 3 hrs.

Max. Marks:100

**Note: Answer FIVE full questions, selecting
at least TWO questions from each part.**

PART – A

- 1 a. Write the truth table of the logic circuit having 3 inputs A, B and C and the output expressed as $Y = \overline{ABC} + ABC$. Also simplify the expression using Boolean algebra and implement the logic circuit using NAND gates. (06 Marks)
- b. Name universal gates. Realize basic gates using NAND gates. (08 Marks)
- c. Explain positive and negative logic. (06 Marks)
- 2 a. Give sum-of-product and product of sum circuit for,
 $f(A, B, C, D) = \sum m(6, 8, 9, 10, 11, 12, 13, 14, 15)$ (08 Marks)
- b. Find essential prime implicants for the Boolean expression by using Quine-McClunsky method.
 $f(W, X, Y, Z) = \sum m(1, 3, 6, 7, 8, 9, 10, 12, 13, 14)$ (12 Marks)
- 3 a. Design a 16 to 1 multiplexer using two 8 to 1 multiplexer and one 2 – to – 1 multiplexer. (06 Marks)
- b. Explain n-bit magnitude comparator. (08 Marks)
- c. Design 7-segments decoder using PLA. (06 Marks)
- 4 a. Explain Schmitt trigger. (06 Marks)
- b. Give state transition diagram of SR, D, JK and T FlipFlops. (08 Marks)
- c. Show how a D Flip-Flop can be converted into JK – Flop Flop. (06 Marks)

PART – B

- 5 a. Design 3-bit PISO (Use D – FlipFlop). (06 Marks)
- b. Design two 4-bit serial adder. (06 Marks)
- c. Design 4-bit Johnson counter with state table. (08 Marks)
- 6 a. Design Synchronous mod 6 up-counter using JK – Flip Flop. (10 Marks)
- b. Explain digital clock with block diagram. (10 Marks)

- 7 a. Reduce state transition diagram (Moore model) Fig. Q7 (a) given below by,
 i) Row elimination method and
 ii) Implication table method, with partition table.

(12 Marks)

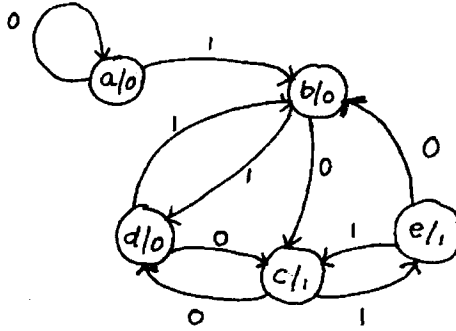


Fig. Q7 (a)

- b. Design an asynchronous sequential logic circuit for state transition diagram shown below Fig. Q7 (b).

(08 Marks)

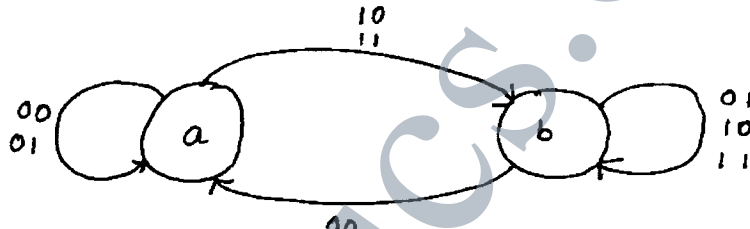


Fig. Q7 (b)

- 8 a. Explain with logic diagram 3-bit simultaneous A/D converters.
 b. Explain with neat diagram, single – slope A/D converter.

(10 Marks)

(10 Marks)
