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10CS33

Third Semester B.E. Degree Examination, June/July 2014

Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Define rise time, fall time in a digital waveform. What is the value of high duty cycle (duty cycle H) if the frequency of a digital waveform is 5 MHz and the width of the positive pulse is 0.05 μs? **(04 Marks)**

b. Realize the basic gates using only NAND gates. **(06 Marks)**

c. What is positive and negative logic? List the equivalences in positive and negative logic. **(04 Marks)**

d. Write a verilog HDL code using structural model for two input AND gate and prepare test-bench to simulate the circuit. Draw the timing diagram generated by simulating the verilog code. Assume 20 ns holding time of each input combination. **(06 Marks)**

2 a. Simplify the Boolean function F(A, B, C, D) = $\sum m(1, 3, 5, 7, 8, 10, 12, 14)$ by using Karnaugh map method and realize the logic circuit using only NAND gates. **(06 Marks)**

b. Draw Karnaugh map of Y = F(A, B, C, D) = $\Pi M(0, 1, 2, 4, 5, 10) \cdot d(8, 9, 11, 12, 13, 15)$ and get the simplified POS form of K-map. **(04 Marks)**

c. Get simplified expression of Y = F(A, B, C, D) = $\sum m(2, 3, 7, 9, 11, 13) + d(1, 10, 15)$ using Quine-McClusky method. **(10 Marks)**

3 a. What is a multiplexer? Design a 4-to-1 multiplexer using logic gates, write the truth table and explain its working principle. **(06 Marks)**

b. Describe the working principle of 3:8 decoder. Design a circuit that realizes the following functions using a 3 : 8 decoder and multi-input OR gates.
$F_1(A, B, C) = \sum m(1, 3, 7)$; $F_2(A, B, C) = \sum m(2, 3, 5)$ **(06 Marks)**

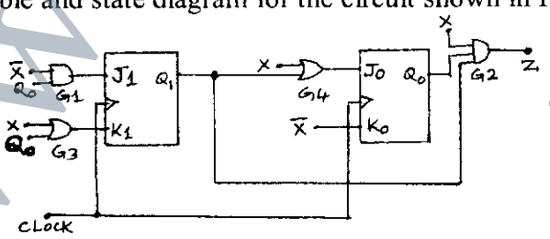
c. What is magnitude comparator? Design one bit comparator and write the truth table, logic circuit using basic gates. **(06 Marks)**

d. How does Programmable Logic Arrays (PLA) differ from a Programmable Array Logic (PAL)? **(02 Marks**

4 a. With the help of neat diagram, explain the working of edge triggered JK flip-flop. Write the state diagram and excitation table. **(06 Marks)**

b. What is switch contact bounce? Explain the working principle of a simple RS latch debounce circuit. **(04 Marks)**

c. Write the state table and state diagram for the circuit shown in Fig.Q4(c).



G_1, G_2 → AND gate
G_3, G_4 → OR gate

Fig.Q4(c) **(10 Marks)**

PART – B

5 a. What is a shift register? Draw the logic diagram of a 4 bit serial in serial out (SISO) shift register using negative edge triggered JK or D flip-flops and explain its operation with the waveform to shift the binary number 1010 into the register. **(08 Marks)**

b. Explain with logic diagram the use of 8-bit SISO shift register in serial addition of two 8-bit numbers. **(08 Marks)**

c. Write verilog HDL code for 4-bit SIPO shift register when all the flip-flop outputs are available externally. **(04 Marks)**

6 a. What are asynchronous and synchronous counters? With a neat block diagram, output waveform and truth table, explain a 3-bit binary ripple counter constructed using negative edge triggered JK flip-flops. **(10 Marks)**

b. Design a mod-5 counter using JK flip-flops having the feature that if an unused state appears, the counter will reset to 000 at the next clock pulse. **(10 Marks)**

7 a. With neat block diagrams compare Mealy model and Moore model of sequential logic system. **(04 Marks)**

b. Draw the ASM chart for the Mealy machine shown in Fig.Q7(b). **(08 Marks)**

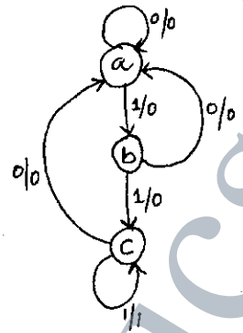


Fig.Q7(b)

c. Using row elimination method reduce the state diagram shown in Fig.Q7(c).

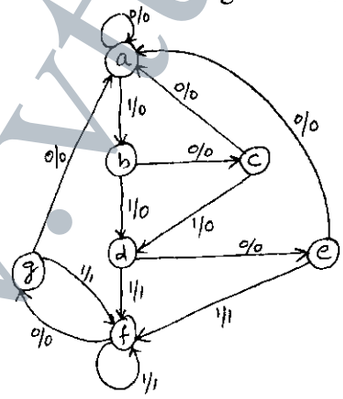


Fig.Q7(c). **(08 Marks)**

8 a. What is the binary ladder? Explain the binary ladder with a digital input of 1000. **(06 Marks)**

b. Define Accuracy and Resolution with respect to DAC. **(04 Marks)**

c. With a neat circuit diagram, explain parallel ADC. **(10 Marks)**

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